IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

WINTERSPRING DIGITAL LLC,	§	
	§	Case No.
Plaintiff,	§	
	§	**JURY TRIAL DEMANDED**
v.	§	
	§	
RENESAS ELECTRONICS CORPORATION,	§	
	§	
Defendant.	§	

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Winterspring Digital LLC ("Winterspring" or "Plaintiff") for its Complaint against Renesas Electronics Corporation ("Renesas" or "Defendant") alleges as follows:

THE PARTIES

1. Winterspring is a limited liability company organized and existing under the laws of the State of Texas, with its principal place of business located at 104 East Houston Street, Marshall, Texas 75670

2. Upon information and belief, Renesas is a Japanese corporation, with a principal place of business located at Toyosu Foresia, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan. Upon information and belief, Renesas does business in Texas and in the Eastern District of Texas, directly or through intermediaries.

JURISDICTION

3. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1, *et seq*. This Court has jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

4. This Court has personal jurisdiction over Defendant. Defendant regularly conducts business and has committed acts of patent infringement and/or has induced acts of patent infringement by others in this Judicial District and/or has contributed to patent infringement by others in this Judicial District, the State of Texas, and elsewhere in the United States.

5. Venue is proper in this Judicial District pursuant to 28 U.S.C. § 1391 because, among other things, Defendant is not a resident in the United States, and thus may be sued in any judicial district pursuant to 28 U.S.C. § 1391(c)(3).

6. Defendant is subject to this Court's jurisdiction pursuant to due process and/or the Texas Long Arm Statute due at least to its substantial business in this State and Judicial District, including (a) at least part of its past infringing activities, (b) regularly doing or soliciting business in Texas, and/or (c) engaging in persistent conduct and/or deriving substantial revenue from goods and services provided to customers in Texas.

PATENTS-IN-SUIT

7. On January 16, 2007, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 7,164,692 (the "'692 Patent") entitled "Apparatus and Method for Transmitting 10 Gigabit Ethernet LAN Signals Over a Transport System." A true and correct copy of the '692 Patent is available at http://pdfpiw.uspto.gov/.piw?docid=7164692.

8. On September 2, 2008, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 7,420,975 (the "'975 Patent") entitled "Method and Apparatus For High-Speed Frame Tagger." A true and correct copy of the '975 Patent is available at http://pdfpiw.uspto.gov/.piw?docid=7420975.

9. On August 10, 2010, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 7,774,468 (the "'468 Patent") entitled "Network Traffic Admission

Control." A true and correct copy of the '468 Patent is available at http://pdfpiw.uspto.gov/.piw?docid=7774468.

10. Winterspring is the sole and exclusive owner of all right, title, and interest in the '692, '975, and '468, Patents (the "Patents-in-Suit") and holds the exclusive right to take all actions necessary to enforce its rights to the Patent-in-Suit, including the filing of this patent infringement lawsuit. Winterspring also has the right to recover all damages for past, present, and future infringement of the Patents-in-Suit and to seek injunctive relief as appropriate under the law.

FACTUAL ALLEGATIONS

11. The Patents-in-Suit generally cover systems and methods for routing data over a network.

12. The '692 Patent generally discloses an apparatus and method for transmitting LAN signals over a transport system. A system sends or receives a signal to or from a transport system, converts the signal to an intermediate form, re-clocks the intermediate signal, reconverts and then transmits the signal. The technology described in the '692 Patent was developed by Jeffrey Lloyd Cox and Samir Satish Seth. By way of example, this technology is implemented today in microchips, SoCs and ASICs the receive, convert, monitor, and send 10-Gigabit LAN signals.

13. The '975 Patent discloses an apparatus and methods for examining a packet, determining a protocol type and tagging the packet. The technology described in the '975 Patent was developed by Velamur Krishnamachari and Dinesh Annayya from Cypress Semiconductor Corporation. By way of example, this technology is implemented today in microchips, SoCs and ASICs which implement packet tagging.

14. The '468 Patent discloses systems and methods for traffic admission control using real time bandwidth allocation. The technology described in the '468 Patent was developed by

Siddhartha Nag, and Srikanth S. Kumar. By way of example, this technology is implemented today in microchips, SoCs, and ASICs that perform traffic admission control using real time bandwidth allocation.

15. Renesas has infringed and is continuing to infringe the Patents-in-Suit by making, using, offering to sell, selling, and/or importing network switches, routers, and software which implement the technology disclosed in the above patents-in-suit.

COUNT I
(Infringement of the '692 Patent)

16. Paragraphs 1 through 15 are incorporated by reference as if fully set forth herein.

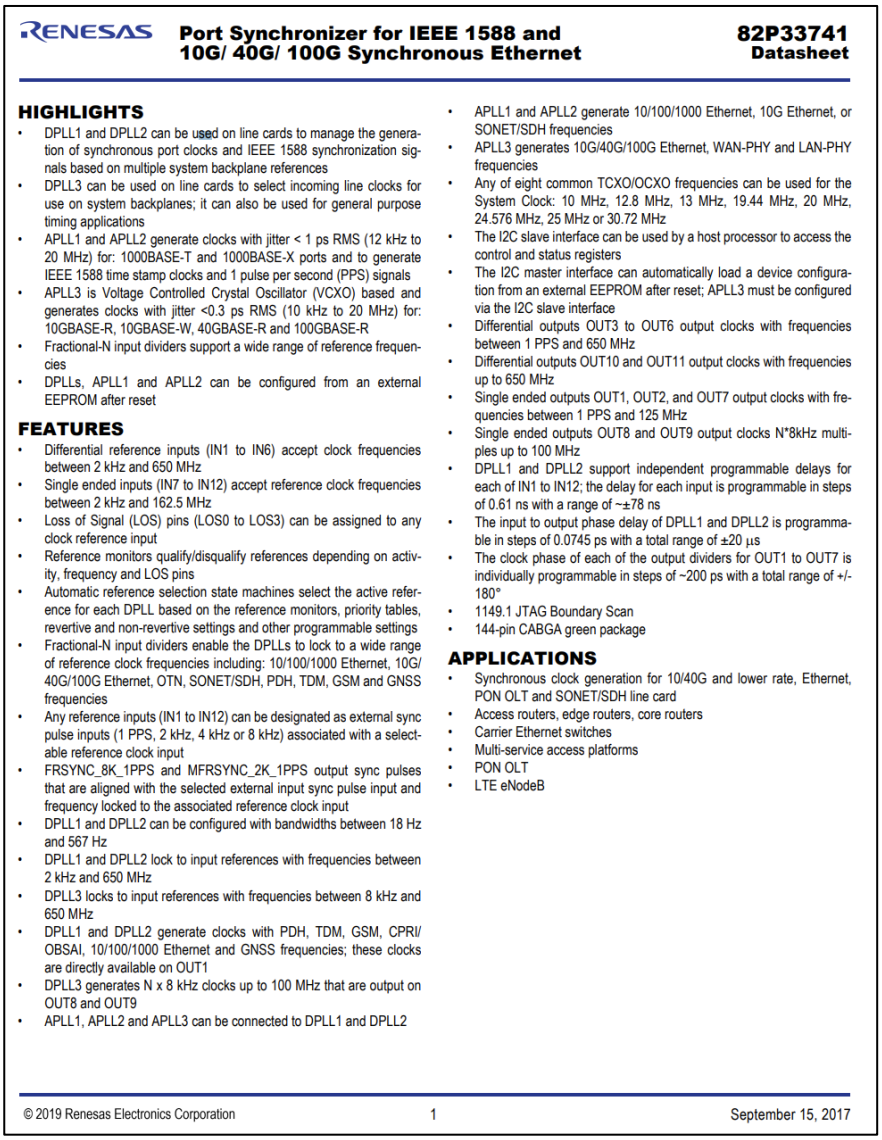
17. Winterspring has not licensed or otherwise authorized Defendant to make, use, offer for sale, sell, or import any products that embody the inventions of the '692 Patent.

18. Defendant has and continues to directly infringe the '692 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States products that satisfy each and every limitation of one or more claims of the '692 Patent. Such products include ethernet Network Adaptors and Controllers, PHYs, ethernet switches, and optical modules, optical interconnects, and network synchronization tools that receive, convert, monitor, and send 10GE LAN signals.

19. For example, Defendant has and continues to directly infringe at least claim 10 of the '692 Patent by making, using, offering to sell, selling, and/or importing into the United States products that receive, convert, and monitor 10GE LAN signals.

20. For example, the Renesas 82P33741 Port Synchronizer performs a method transferring 10GE LAN client signals from a transport system to a client system comprising receiving the 10GE LAN client signal transmitted over the transport system, converting the 10GE

LAN client signal to an intermediate signal, recovering clock data from the intermediate signal, recovering a data stream from the intermediate signal, reconverting the intermediate signal to the 10GE LAN client signal; transferring the 10GE LAN client signal to a client system; and monitoring the intermediate form with a monitoring device wherein the monitoring device is a 10GE LAN media access controller.



RENESAS

Port Synchronizer for IEEE 1588 and 10G/ 40G/ 100G Synchronous Ethernet

82P33741 Datasheet

HIGHLIGHTS

- DPLL1 and DPLL2 can be used on line cards to manage the generation of synchronous port clocks and IEEE 1588 synchronization signals based on multiple system backplane references
- DPLL3 can be used on line cards to select incoming line clocks for use on system backplanes; it can also be used for general purpose timing applications
- APLL1 and APLL2 generate clocks with jitter < 1 ps RMS (12 kHz to 20 MHz) for: 1000BASE-T and 1000BASE-X ports and to generate IEEE 1588 time stamp clocks and 1 pulse per second (PPS) signals
- APLL3 is Voltage Controlled Crystal Oscillator (VCXO) based and generates clocks with jitter <0.3 ps RMS (10 kHz to 20 MHz) for: 10GBASE-R, 10GBASE-W, 40GBASE-R and 100GBASE-R
- Fractional-N input dividers support a wide range of reference frequencies
- DPLLs, APLL1 and APLL2 can be configured from an external EEPROM after reset

FEATURES

- Differential reference inputs (IN1 to IN6) accept clock frequencies between 2 kHz and 650 MHz
- Single ended inputs (IN7 to IN12) accept reference clock frequencies between 2 kHz and 162.5 MHz
- Loss of Signal (LOS) pins (LOS0 to LOS3) can be assigned to any clock reference input
- Reference monitors qualify/disqualify references depending on activity, frequency and LOS pins
- Automatic reference selection state machines select the active reference for each DPLL based on the reference monitors, priority tables, revertive and non-revertive settings and other programmable settings
- Fractional-N input dividers enable the DPLLs to lock to a wide range of reference clock frequencies including: 10/100/1000 Ethernet, 10G/ 40G/100G Ethernet, OTN, SONET/SDH, PDH, TDM, GSM and GNSS frequencies
- Any reference inputs (IN1 to IN12) can be designated as external sync pulse inputs (1 PPS, 2 kHz, 4 kHz or 8 kHz) associated with a selectable reference clock input
- FRSYNC_8K_1PPS and MFRSYNC_2K_1PPS output sync pulses that are aligned with the selected external input sync pulse input and frequency locked to the associated reference clock input
- DPLL1 and DPLL2 can be configured with bandwidths between 18 Hz and 567 Hz
- DPLL1 and DPLL2 lock to input references with frequencies between 2 kHz and 650 MHz
- DPLL3 locks to input references with frequencies between 8 kHz and 650 MHz
- DPLL1 and DPLL2 generate clocks with PDH, TDM, GSM, CPRI/ OBSAI, 10/100/1000 Ethernet and GNSS frequencies; these clocks are directly available on OUT1
- DPLL3 generates N x 8 kHz clocks up to 100 MHz that are output on OUT8 and OUT9
- APLL1, APLL2 and APLL3 can be connected to DPLL1 and DPLL2
- APLL1 and APLL2 generate 10/100/1000 Ethernet, 10G Ethernet, or SONET/SDH frequencies
- APLL3 generates 10G/40G/100G Ethernet, WAN-PHY and LAN-PHY frequencies
- Any of eight common TCXO/OCXO frequencies can be used for the System Clock: 10 MHz, 12.8 MHz, 13 MHz, 19.44 MHz, 20 MHz, 24.576 MHz, 25 MHz or 30.72 MHz
- The I2C slave interface can be used by a host processor to access the control and status registers
- The I2C master interface can automatically load a device configuration from an external EEPROM after reset; APLL3 must be configured via the I2C slave interface
- Differential outputs OUT3 to OUT6 output clocks with frequencies between 1 PPS and 650 MHz
- Differential outputs OUT10 and OUT11 output clocks with frequencies up to 650 MHz
- Single ended outputs OUT1, OUT2, and OUT7 output clocks with frequencies between 1 PPS and 125 MHz
- Single ended outputs OUT8 and OUT9 output clocks N*8kHz multiples up to 100 MHz
- DPLL1 and DPLL2 support independent programmable delays for each of IN1 to IN12; the delay for each input is programmable in steps of 0.61 ns with a range of ~±78 ns
- The input to output phase delay of DPLL1 and DPLL2 is programmable in steps of 0.0745 ps with a total range of ±20 µs
- The clock phase of each of the output dividers for OUT1 to OUT7 is individually programmable in steps of ~200 ps with a total range of +/- 180°
- 1149.1 JTAG Boundary Scan
- 144-pin CABGA green package

APPLICATIONS

- Synchronous clock generation for 10/40G and lower rate, Ethernet, PON OLT and SONET/SDH line card
- Access routers, edge routers, core routers
- Carrier Ethernet switches
- Multi-service access platforms
- PON OLT
- LTE eNodeB

[1]

[1] "Renesas Port Synchronizer for IEEE 1588 and 10G/40G/100G Synchronous Ethernet: Datasheet" at Pg. 1. Available at: https://www.renesas.com/us/en/document/dst/82p33741-datasheet?r=117281.

21. Defendant has and continues to indirectly infringe one or more claims of the ’692 Patent by knowingly and intentionally inducing others, including Renesas customers and end-users, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling and/or importing into the United States microchips, SoCs, ASICs and other products that receive, convert, monitor, and send 10GE LAN signals.

22. Defendant, with knowledge that these products, or the use thereof, infringe the ’692 Patent at least as of the date of this Complaint, knowingly and intentionally induced, and continues to knowingly and intentionally induce, direct infringement of the ’692 Patent by providing these products to end users for use in an infringing manner.

23. Defendant induced infringement by others, including end users, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability that others, including end users, infringe the ’692 Patent, but while remaining willfully blind to the infringement.

24. Winterspring has suffered damages as a result of Defendant’s direct and indirect infringement of the ’692 Patent in an amount to be proved at trial.

25. Winterspring has suffered, and will continue to suffer, irreparable harm as a result of Defendant’s infringement of the ’692 Patent, for which there is no adequate remedy at law, unless Defendant’s infringement is enjoined by this Court.

COUNT II
(Infringement of the ’975 Patent)

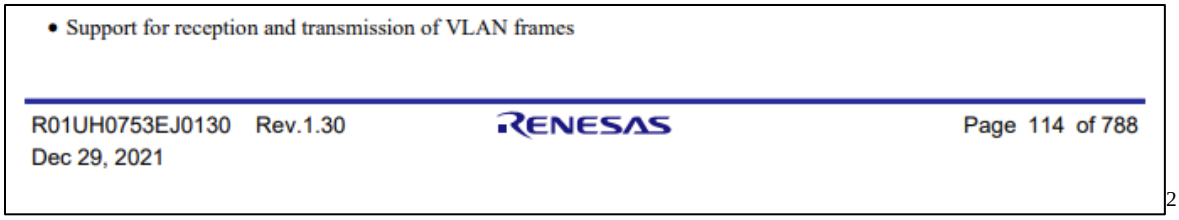
26. Paragraphs 1 through 15 are incorporated by reference as if fully set forth herein.

27. Winterspring has not licensed or otherwise authorized Defendant to make, use, offer for sale, sell, or import any products that embody the inventions of the ’975 Patent.

28. Defendant has and continues to directly infringe the ’975 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States products that satisfy each and every limitation of one or more claims of the ’975 Patent. Such products include but are not limited to network adaptors and controllers and ethernet switches that perform packet tagging.

29. For example, Defendant has and continues to directly infringe at least claim 5 of the ’975 Patent by making, using, offering to sell, selling, and/or importing into the United States products that perform packet tagging:

30. For example, the Renesas RZ/N1D includes an apparatus comprising a network processor interface suitable for coupling to a network processor and a central processor interface suitable for coupling to a central processor. Upon information and belief, the Renesas RZ/N1D further includes a protocol determination logic block to determine a protocol type of data in a packet, wherein the protocol determination logic compares the protocol information in a first pass to predetermined values to procedure a first result and, if the first result is positive, compares the protocol information in a second pass to predetermined values to produce a second result, the first and second results forming a set of results. Upon information and belief, the Renesas RZ/N1D further comprises a tag select logic block to apply a tag to the packet indicating that the packet has an unknown protocol type if the first result is negative and if the first result is positive, the packet should be sent to either the central processor interface or the network processor interface based on the set of results.



- Support for reception and transmission of VLAN frames

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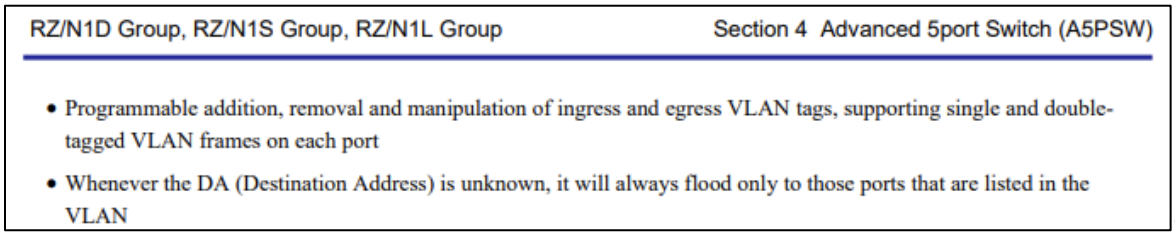
[2]



RZ/N1D Group, RZ/N1S Group, RZ/N1L Group Section 4 Advanced 5port Switch (A5PSW)

- Programmable addition, removal and manipulation of ingress and egress VLAN tags, supporting single and double-tagged VLAN frames on each port
- Whenever the DA (Destination Address) is unknown, it will always flood only to those ports that are listed in the VLAN

[3]

31. Defendant has and continues to indirectly infringe one or more claims of the ’975 Patent by knowingly and intentionally inducing others, including Renesas customers and end-users, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling and/or importing into the United States products that include microchips, SoCs, ASICs and other products that implement packet tagging.

32. Defendant, with knowledge that these products, or the use thereof, infringed the ’975 Patent at least as of the date of this Complaint, knowingly and intentionally induced, and continues to knowingly and intentionally induce, direct infringement of the ’975 Patent by providing these products to end users for use in an infringing manner.

33. Defendant induced infringement by others, including end users, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability

[2] “Renesas RZ/N1D Group, RZ/N1S Group, RZ/N1L Group User Manual: R-IN Engine and Ethernet Peripherals: User Manual” at. Pg. 114. Available at: https://www.renesas.com/us/en/document/mah/rzn1d-group-rzn1s-group-rzn1l-group-users-manual-r-engine-and-ethernet-peripherals?language=en.

[3] “Renesas RZ/N1D Group, RZ/N1S Group, RZ/N1L Group User Manual: R-IN Engine and Ethernet Peripherals: User Manual” at. Pg. 114. Available at: https://www.renesas.com/us/en/document/mah/rzn1d-group-rzn1s-group-rzn1l-group-users-manual-r-engine-and-ethernet-peripherals?language=en.

that others, including end users, infringe the ’975 Patent, but while remaining willfully blind to the infringement.

34. Winterspring has suffered damages as a result of Defendant’s direct and indirect infringement of the ’975 Patent in an amount to be proved at trial.

35. Winterspring has suffered, and will continue to suffer, irreparable harm as a result of Defendant’s infringement of the ’975 Patent, for which there is no adequate remedy at law, unless Defendant’s infringement is enjoined by this Court.

COUNT III
(Infringement of the ’468 Patent)

36. Paragraphs 1 through 15 are incorporated by reference as if fully set forth herein.

37. Winterspring has not licensed or otherwise authorized Defendant to make, use, offer for sale, sell, or import any products that embody the inventions of the ’468 Patent.

38. Defendant has and continues to directly infringe the ’468 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States products that satisfy each and every limitation of one or more claims of the ’468 Patent. Such products include but are not limited to network adaptors and controllers and ethernet switches which allow for traffic admission control using real time bandwidth allocation.

39. For example, Defendant has and continues to directly infringe at least claim 1 of the ’468 Patent by making, using, offering to sell, selling, and/or importing into the United States products that hardware and software which allow for traffic admission control using real time bandwidth allocation.

40. For example, the Renesas 89TTM552 Traffic Manager performs a method of a first edge node requesting from a director node, an amount of bandwidth over a first of a plurality of

paths in a network between the first edge node and a second edge node, wherein the director node is configured to maintain information indicative of bandwidth available along each of the plurality of paths. Upon information and belief, in response to the requested amount of bandwidth being available along the first path, the Renesas 89TTM552 Traffic Manager performs the step of the first edge node receiving, from the director node, an allocation of bandwidth as a real-time bandwidth pool associated with network resources in the first path. Upon information and belief, the Renesas 89TTM552 Traffic Manager performs the step of the first edge node receiving a connection request to establish a first real-time communication session between one of a first plurality of communication devices coupled to the first edge node and one of a second plurality of communication devices coupled to the second edge node. Upon information and belief, in response to determining that network resources in the real-time bandwidth pool are available to permit communication over the first path, the Renesas 89TTM552 Traffic Manager performs the step of the first edge node responding to the connection request by allocating a portion of the real-time bandwidth pool to the first real-time communication session.

RENESAS **Traffic Manager Data Sheet** ***89TTM552***

Preliminary Information*

Description

The 89TTM55x Traffic Manager chipset consists of a 89TTM552 aggregate-flow device and a 89TTM553 per-flow device. The 89TTM55x Traffic Manager manages bandwidth resources by shaping traffic to defined rate profiles and by precisely controlling the allocation of bandwidth and acceptance of new traffic during times of network congestion. The 89TTM55x provides a full suite of configurable algorithms that support quality of service differentiation for any data protocol, at line rates of 10 Gbps.

The 89TTM552, which can operate as a standalone device, is a 10 Gbps simplex device providing the following features:

- *An aggregate-flow (AFQ) scheduler that can be used for class-based, virtual pipe, or flow scheduling for up to 4K queues.*
- *A logical port scheduler (1K port queues).*
- *Output queuing for channel-based backpressure from a framer or fabric (1K OQs).*
- *Supports up to 256 MB external data buffering.*
- *Sophisticated congestion management features to manage buffer resources.*
- *Spatial multicast labeling for the switch fabric and logical multicasting.*
- *Packet segmentation and reassembly across fabric or SPI4.2 channels.*
- *AAL-5 segmentation and reassembly.*

The 89TTM552 can be used in standalone mode to handle congestion management and scheduling of traffic where three levels of hierarchy and 4K queues (AFQs) are sufficient.

The 89TTM552 can perform simultaneous scheduling of a large number of flows, each at an individual rate of fine granularity, and with many user-configurable features allowing maximum flexibility and performance. It has congestion management mechanisms that manage shared traffic buffering resources. If buffer memory approaches its limit because data arrives at a queue faster than it can depart, the 89TTM552 performs per-queue congestion management. It can also intelligently discard lower priority traffic as it arrives until memory resources become available.

The 89TTM552 controls traffic forwarding, manages the shared buffer resources with multi-level thresholding, maintains the various queues, and generates queue service selections (scheduling for departures) using bandwidth management algorithms developed by IDT. Using industry-standard 16-bit LVDS Rx and Tx interfaces, the 89TTM552 receives and transmits data as packets or cells.

The 89TTM552 manages its data storage internally. It has fixed blocks of memory for storing and forwarding data, and for managing memory resources according to quality of service parameters. Each block, or cell, contains up to 64 bytes of data payload from a packet. The 89TTM552 can process up to 35 Mcps/Mpps for both arrivals and departures. The 89TTM552 and 89TTM553 both operate up to 175 MHz.

[4]

IDT 89TTM552

The 89TTM552 connects seamlessly to IDT's 89TSF family of switch fabric products. It can also operate seamlessly with network processors and switch fabrics that use one of its 16-bit LVDS interface protocols. The 89TTM552 can also directly transmit to third-party framers/PHYs that have SPI4.2 interfaces.

The 89TTM553 consists of a flow-based available-rate scheduler with a weighted fair queuing (WFQ) engine and adds support for further hierarchical scheduling with queues for up to 1M flows. Both devices, the 89TTM552 and 89TTM553, are used when additional hierarchical scheduling and a large number of simultaneous flows are required. See Figure 1 for a functional diagram of the 89TTM55x chipset.

[5]

[4] "Renesas 89TTM552 Traffic Manager Data Sheet" at. Pg. 1. Available at: https://www.renesas.com/us/en/document/dst/89ttm552-traffic-manager-data-sheet.
[5] *Id*. at 2.

41. Defendant has and continues to indirectly infringe one or more claims of the '468 Patent by knowingly and intentionally inducing others, including Renesas customers and end-users, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling and/or importing into the United States products that include microchips, SoCs, ASICs and other products which allow for traffic admission control using real time bandwidth allocation.

42. Defendant, with knowledge that these products, or the use thereof, infringe the '468 Patent at least as of the date of this Complaint, knowingly and intentionally induced, and continues to knowingly and intentionally induce, direct infringement of the '468 Patent by providing these products to end users for use in an infringing manner.

43. Defendant induced infringement by others, including end users, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability that others, including end users, infringe the '468 Patent, but while remaining willfully blind to the infringement.

44. Winterspring has suffered damages as a result of Defendant's direct and indirect infringement of the '468 Patent in an amount to be proved at trial.

45. Winterspring has suffered, and will continue to suffer, irreparable harm as a result of Defendant's infringement of the '468 Patent, for which there is no adequate remedy at law, unless Defendant's infringement is enjoined by this Court.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury for all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, Winterspring prays for relief against Defendant as follows:

a. Entry of judgment declaring that Defendant has directly and/or indirectly infringed one or more claims of the Patents-in-Suit;

b. An order pursuant to 35 U.S.C. § 283 permanently enjoining Defendant, its officers, agents, servants, employees, attorneys, and those persons in active concert or participation with it, from further acts of infringement of one or more of the Patents-in-Suit;

c. An order awarding damages sufficient to compensate Winterspring for Defendant's infringement of the Patents-in-Suit, but in no event less than a reasonable royalty, together with interest and costs;

d. Entry of judgment declaring that this case is exceptional and awarding Winterspring its costs and reasonable attorney fees under 35 U.S.C. § 285; and,

e. Such other and further relief as the Court deems just and proper.

Dated: January 23, 2023

Respectfully submitted,

/s/ Vincent J. Rubino, III

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